1. A clock synchronizer circuit to provide an internal clock signal for an integrated circuit that is synchronized to an external system clock signal, such that said internal clock signal is aligned with and has minimal skew from said external system clock signal, whereby said clock synchronizer circuit is comprising:

a plurality of serially connected delaying means to receive said external system clock signal and delay said external system clock signal by an incremental period of delay;

a plurality of frequency divider means, whereby a first frequency divider means receives said external system clock signal and divides a frequency of said external system clock signal by a dividing factor and each remaining frequency divider means is connected to an output of one of the serially connected delaying means to divide a delayed external system clock signal by said dividing factor providing a plurality of divided external system clock signals;

a plurality of clock synchronization delay means, whereby each clock synchronization delay means is connected to one of the plurality of frequency divider means to synchronized each divided external system clock signal to the external system clock signal; and

a logical combining means to combine the synchronize, divided external system clock signals to form said internal clock signal.

2. The clock synchronizer circuit of claim 1 wherein said incremental period of delay is equal to a period of one cycle of said external system clock signal.

3. The clock synchronizer circuit of claim 1 wherein the number serially connected delaying means is one less than said dividing factor.

4. The clock synchronizer circuit of claim 1 wherein the number of frequency divider means is equal to the dividing factor.

5. The clock synchronizer circuit of claim 1 wherein each clock synchronization delay means is a synchronous mirror delay circuit.

6. The clock synchronizer circuit of claim 5 wherein the synchronous mirror delay circuit is comprising:

a buffer circuit connected to one of the frequency divider means to buffer, amplify and delay one of the delayed and divided external timing signals to create a first timing signal;

a fixed delay circuit connected to the buffer circuit to delay the first timing signal by a circuit delay factor that is a sum of a first delay factor and a second delay factor, whereby said first delay factor is a delay time of the frequency divider means and the buffer circuit;

a forward delay circuit to measure a difference time period that is the circuit delay factor subtracted from the period of the delayed and divided external timing signal;

a mirror delay circuit connected to the forward delay circuit and the buffer circuit to delay the first timing signal by the difference time period to create a second timing signal; and

an internal buffer circuit connected to the mirror delay circuit to amplify, delay the second timing signal to create the synchronized, divided external system clock signal whereby a delay time of said internal buffer circuit is the second delay factor.

7. The clock synchronizer circuit of claim 1 wherein said integrated circuit is a synchronous dynamic random access memory and said internal clock controls a transfer of digital data to and from said synchronous dynamic random access memory.

8. The clock synchronizer circuit of claim 1 wherein the dividing factor is two.

9. The clock synchronizer circuit of claim 8 wherein the internal clock signal is synchronized with the external system clock signal after four periods of said external system clock signal.

10. A clock synchronizer circuit to provide an internal clock signal for an integrated circuit that is synchronized to an external system clock signal, such that said internal clock signal is aligned with and has minimal skew from said external system clock signal, whereby said clock synchronizer circuit is comprising:

a frequency divider means that receives said external system clock signal and divides its frequency by a dividing factor to form a divided external clock signal;

a plurality of serially connected delaying means, whereby a first delaying means is connected to the frequency divider means to receive the divided external clock signal, and each delaying means delays said delayed external clock signal by an incremental period of delay to form a plurality of delayed and divided external clock signals.;

a plurality of clock synchronization delay means, whereby a first clock synchronization delay means is connected to frequency divider means and each remaining clock synchronization delay means is connected to one of the plurality of serially connected delaying means to synchronize each delayed and divided external clock signal to the external system clock signal; and

a logical combining means to combine the synchronized, delayed and divided external clock signals to form said internal clock signal.

11. The clock synchronizer circuit of claim 10 wherein said incremental period of delay is equal to a period of one cycle of said external system clock signal.

12. The clock synchronizer circuit of claim 10 wherein the number serially connected delaying means is one less than said dividing factor.

13. The clock synchronizer circuit of claim 10 wherein each clock synchronization delay means is a synchronous mirror delay circuit.

14. The clock synchronizer circuit of claim 13 wherein the synchronous mirror delay circuit is comprising:

a buffer circuit connected to one of the frequency divider means to buffer, amplify and delay one of the delayed and divided external timing signals to create a first timing signal;

a fixed delay circuit connected to the buffer circuit to delay the first timing signal by a circuit delay factor that is a sum of a first delay factor and a second delay factor, whereby said first delay factor is a delay time of the frequency divider means and the buffer circuit;

a forward delay circuit to measure a difference time period that is the circuit delay factor subtracted from the period of the delayed and divided external timing signal;

a mirror delay circuit connected to the forward delay circuit and the buffer circuit to delay the first timing signal by the difference time period to create each synchronized, delayed and divided external clock signal; and

an internal buffer circuit connected to the logical combining means to amplify and delay the internal clock signal whereby a delay time of said internal buffer circuit and the logical combining means is the second delay factor.

15. The clock synchronizer circuit of claim 10 wherein said integrated circuit is a synchronous dynamic random access memory and said internal clock controls a transfer of digital data to and from said synchronous dynamic random access memory.

16. The clock synchronizer circuit of claim 10 wherein the dividing factor is two.

17. The clock synchronizer circuit of claim 16 wherein the internal clock signal is synchronized with the external system clock signal after four periods of said external system clock signal.

18. A synchronous dynamic random access memory to retain digital data, comprising:

a clock generator circuit connected between an external system clock distribution circuit and a plurality of banks of arrays of memory cells, an address circuit, a command circuit, a data control circuit, and a data input/output buffer to provide a timing signal to synchronize operation of said synchronous dynamic random access memory, whereby certain operations must occur in time with minimal deviation from said an external system clock signal and whereby said clock generator includes at least one clock synchronizer circuit, comprising;

a plurality of serially connected delaying means to receive said external system clock signal and delay said external system clock signal by an incremental period of delay;

a plurality of frequency divider means, whereby a first frequency divider means receives said external system clock signal and divides a frequency of said external system clock signal by a dividing factor and each remaining frequency divider means is connected to an output of one of the serially connected delaying means to divide a delayed external system clock signal by said dividing factor providing a plurality of divided external system clock signals;

a plurality of clock synchronization delay means, whereby each clock synchronization delay means is connected to one of the plurality of frequency divider means to synchronized

each divided external system clock signal to the external system clock signal; and

a logical combining means to combine the synchronized, divided external system clock signal to form said internal clock signal.

19. The clock synchronizer circuit of claim 18 wherein said incremental period of delay is equal to a period of one cycle of said external system clock signal.

20. The clock synchronizer circuit of claim 18 wherein the number serially connected delaying means is one less than said dividing factor.

21. The clock synchronizer circuit of claim 18 wherein the number of frequency divider means is equal to the dividing factor.

22. The clock synchronizer circuit of claim 18 wherein each clock synchronization delay means is a synchronous mirror delay circuit.

23. The clock synchronizer circuit of claim 22 wherein the synchronous mirror delay circuit is comprising:

a buffer circuit connected to one of the frequency divider means to buffer, amplify and delay one of the delayed and divided external timing signals to create a first timing signal;

a fixed delay circuit connected to the buffer circuit to delay the first timing signal by a circuit delay factor that is a sum of a first delay factor and a second delay factor, whereby said first delay factor is a delay time of the frequency divider means and the buffer circuit;

a forward delay circuit to measure a difference time period that is the circuit delay factor subtracted from the period of the delayed and divided external timing signal;

a mirror delay circuit connected to the forward delay circuit and the buffer circuit to delay the first timing signal by the difference time period to create a second timing signal; and

an internal buffer circuit connected to the mirror delay circuit to amplify, delay the second timing signal to create the internal clock signal whereby a delay time of said internal buffer circuit is the second delay factor.

24. The clock synchronizer circuit of claim 18 wherein said integrated circuit is a synchronous dynamic random access memory and said internal clock controls a transfer of digital data to and from said synchronous dynamic random access memory.

25. The clock synchronizer circuit of claim 18 wherein the dividing factor is two.

26. The clock synchronizer circuit of claim 26 wherein the internal clock signal is synchronized with the external system clock signal after four periods of said external system clock signal.

27. A synchronous dynamic random access memory to retain digital data, comprising:

a clock generator circuit connected between an external system clock distribution circuit and a plurality of banks of arrays of memory cells, an address circuit, a command circuit, a data control circuit, and a data input/output buffer to provide a timing signal to synchronize operation of said synchronous dynamic random access memory, whereby certain operations must occur in time with minimal deviation from said an external system clock signal and whereby said clock generator includes at least one clock synchronizer circuit, comprising;

a frequency divider means that receives said external system clock signal and divides its frequency by a dividing factor to form a divided external clock signal;

a plurality of serially connected delaying means, whereby a first delaying means is connected to the frequency divider

means to receive the divided external clock signal, and each delaying means delays said delayed external clock signal by an incremental period of delay to form a plurality of delayed and divided external clock signals.;

a plurality of clock synchronization delay means, whereby a first clock synchronization delay means is connected to frequency divider means and each remaining clock synchronization delay means is connected to one of the plurality of serially connected delaying means to synchronize each delayed and divided external clock signal to the external system clock signal; and

a logical combining means to combine the synchronized, delayed and divided external clock signals to form said internal clock signal.

28. The clock synchronizer circuit of claim 27 wherein said incremental period of delay is equal to a period of one cycle of said external system clock signal.

29. The clock synchronizer circuit of claim 27 wherein the number serially connected delaying means is one less than said dividing factor.

30. The clock synchronizer circuit of claim 27 wherein each clock synchronization delay means is a synchronous mirror delay circuit.

31. The clock synchronizer circuit of claim 30 wherein the synchronous mirror delay circuit is comprising:

a buffer circuit connected to one of the frequency divider means to buffer, amplify and delay one of the delayed and divided external timing signals to create a first timing signal;

a fixed delay circuit connected to the buffer circuit to delay the first timing signal by a circuit delay factor that is a sum of a first delay factor and a second delay factor, whereby said first delay factor is a delay time of the frequency divider means and the buffer circuit;

a forward delay circuit to measure a difference time period that is the circuit delay factor subtracted from the period of the delayed and divided external timing signal;

a mirror delay circuit connected to the forward delay circuit and the buffer circuit to delay the first timing signal by the difference time period to create each synchronized, delayed and divided external clock signal; and

an internal buffer circuit connected to the logical combining means to amplify and delay the internal clock signal whereby a delay time of said internal buffer circuit and the logical combining means is the second delay factor.

32. The clock synchronizer circuit of claim 27 wherein said integrated circuit is a synchronous dynamic random access memory and said internal clock controls a transfer of digital data to and from said synchronous dynamic random access memory.

33. The clock synchronizer circuit of claim 27 wherein the dividing factor is two.

34. The clock synchronizer circuit of claim 33 wherein the internal clock signal is synchronized with the external system clock signal after four periods of said external system clock signal.

35. A method for generating an internal clock signal for an integrated circuit that is synchronized to an external system clock, such that said internal clock signal is aligned with and has minimal skew from said external system clock signal whereby said method is comprising the steps of:

acquiring said external system clock signal;

generating a plurality of delayed, submultiple clock signals;

synchronizing by delaying each of said plurality of delayed submultiple clock signals to the external system clock to form a plurality of synchronized submultiple clocks; and

logically combining said plurality of synchronized submultiple clocks to form the internal clock.

36. The method of claim 35 wherein generating the plurality of delayed, submultiple clock signals; by the steps of:

dividing a frequency of the external system clock by a dividing factor, and

delaying each of said divided system clock signals sequentially by an incremental amount;

37. The method of claim 35 wherein generating the plurality of delayed, submultiple clock signals; by the steps of:

delaying each of said external system clock signals sequentially by an incremental amount to form a plurality of delayed external system clock signals; and

dividing a frequency of the plurality of delayed external system clock signals by a dividing factor.

38. The method of claim 37 wherein the incremental amount is equal to a period of the external system clock.

39. The method of claim 38 wherein the incremental amount is equal to a period of the external system clock.

40. The method of claim 35 wherein the number of delayed submultiple clock signals is equal to the dividing factor

41. The method of claim 35 wherein synchronizing by delaying comprises the steps of:

generating a first timing signal by the steps of buffering, amplifying and delaying said delayed submultiple clock;

generating a second timing signal by the step of delaying the first timing signal by a fixed delay factor, whereby said fixed delay factor is a sum of a first delay factor and a second delay factor, wherein said first delay factor is a time required for generating said first timing signal and said second timing signal;

measuring a difference time between the period of the first timing signal and the fixed delay factor

generating a third timing signal by the step of delaying the first timing signal by said difference time; and

generating each synchronized submultiple clock by the steps of delaying the second timing signal by the second delay factor and amplifying said delayed second timing signal.

42. The method of claim 35 wherein said integrated circuit is a synchronous dynamic random access memory and said internal clock controls a

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transfer of digital data to and from said synchronous dynamic random access memory.

43. The method of claim 36 wherein the number of delayed, submultiple clocks is two.

44. The method of claim 37 wherein the delayed, submultiple clocks is two.

45. The method of claim 43 wherein the internal clock signal is synchronized with the external system clock signal after four periods of said external system clock.

46. The method of claim 44 wherein the internal clock signal is synchronized with the external system clock signal after four periods of said external system clock.

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